This listing of claims will replace all prior versions, and listings, of claims in the application:

The Status of the Claims

1-11 (Cancelled)

12. (Currently Amended) A metal line structure formed in a semiconductor device, comprising:

first metal lines formed on a substrate, the first metal lines having a first barrier metal layer and a first conductive layer;

a first interlayer insulator between adjacent ones of the first metal lines;

second metal lines formed on respective ones of the first metal lines, the second metal lines having a second barrier metal layer and a second conductive layer; and

a second interlayer insulator between adjacent ones of the second metal lines[[.]];

wherein the first conductive layer is formed of a material different from a material of the second conductive layer, and the second metal lines prevent ions of the first metal lines from being diffused into the substrate.

13. (Currently Amended) A metal line structure as defined in claim 12, wherein each of the first metal lines has ~~about 50% of a desired~~ a thickness substantially identical to a thickness of the second metal ~~line structure~~lines.

14. (Currently Amended) A metal line structure as defined in claim 12, wherein the first ~~metal lines comprises~~ conductive layer is formed of an Al alloy

containing ~~not~~ greater than 5% ~~or less~~Cu.

15. (Currently Amended) A metal line structure as defined in claim 12, wherein the ~~second~~ first interlayer insulator has ~~about 50% of~~ a ~~desired~~ thickness substantially identical to a thickness of the ~~desired metal line structure~~second interlayer insulator.

16. (Currently Amended) A metal line structure as defined in claim 12, wherein the second conductive layer ~~comprises~~ is substantially formed of Cu.

17. (Currently Amended) A metal line structure as defined in claim 12, wherein the first interlayer insulator is made of ~~USG~~undoped silicate glass (USG) or ~~FSG~~fluorinated silicate glass (FSG) deposited by ~~an HDP~~a high density plasma (HDP) process.

18. (Currently Amended) A metal line structure as defined in claim 12, wherein the second interlayer insulator is made of ~~USG~~undoped silicate glass (USG) or ~~FSG~~fluorinated silicate glass (FSG) deposited by a ~~PECVD~~plasma enhanced chemical vapor deposition (PECVD) process.

19. (Currently Amended) A metal line structure as defined in claim 12, wherein the second interlayer insulator is made of ~~USG~~undoped silicate glass (USG), [[or]] ~~FSG~~fluorinated silicate glass (FSG), or SiOC deposited by a ~~PECVD SIOC~~plasma enhanced chemical vapor deposition (PECVD) ~~SiOC~~ process.

20. (Original) A metal line structure as defined in claim 12, wherein the first and the second barrier metal layers comprise at least one of Ti, TiN, Ta, TaN, W and WN.

Please enter the following new claim:

21. (New) A metal line structure as defined in claim 12, wherein the first conductive layer and the first interlayer insulator are deposited by a plating process.